Remarks

This paper is a reply to the Office Action mailed November 15, 2004 as paper number 7. Claims 1-27 were pending in the application and stand rejected. In this response, claims 1-5, 7, 10-14, 16, 19-27 are currently amended. New claims 28-39 are added to more completely claim the invention. Reconsideration of the application is requested.

1. Section 112, second paragraph

Claims 4, 13 and 22 were rejected under Section 112, second paragraph. The present amendments to these claims are believed to obviate these rejections. For example, in claim 1, the term "state metric" is now used to unambiguously refer to the value selected based on the saturation condition; either the first path metric value (sum) or a predetermined maximum value. The "state metric" term finds support in the specification at page 53, line 20 – page 54, line 1 ("state metric accumulators"); and page 54, last paragraph, to page 55, line 2: "An ACS comparator unit 1620 then selects the path with the smallest *state metric*, and the updated *state metric* is saved into the state accumulator 1610." Corresponding changes are made for consistency in claims 2-4. The "state metric" term is also adopted in claim 10, with corresponding changes in dependent claims 11-16.

2. Informalities

Claims 5, 14 and 23 were objected to because of certain informalities. These are corrected by present amendments as required by the Examiner.

3. *Bree et al.* does not anticipate the present invention.

Claims 1-5, 10-14 and 19-23 were rejected as anticipated by *Bree et al.* (IEEE 1988). Applicant respectfully traverses these grounds for rejection and requests reconsideration in view of the foregoing amendments to the claims and the comments below.

Bree et al. (hereinafter simply "Bree") disclose a bit-serial architecture for a Viterbi type of processor. While Bree recognizes a path metric overflow problem, he discloses a very different solution from the present invention. Bree teaches: "Normalization is done by

clearing the output of a resettable D-type flip-flop which is used as the MSB of the PMV [path metric value] shift register." Page 75, column 2, "PMV Normalization".

The present invention, by contrast, includes at least three important features, individually and in combination, none of which are disclosed in Bree. Briefly, these pertain to: (1) forcing saturation responsive to adder overflow in the ACS circuitry; (2) normalizing the path metric accumulators by inserting normalizing values *into the branch metric calculations*; and (3) providing for dynamic selection among multiple different normalization values. Each of these novel aspects of the invention is discussed in turn.

1. Saturation Logic

Claims 1-27 relate to saturation of the branch metric adders in a decoder. While Bree mentions *accumulator normalization* (discussed below), there is no disclosure about branch metric adder saturation; it is a different problem. Even if one considers "normalization" as a solution to address "overflow" or "saturation" of a circuit, claims 1-27 relate to saturation in the branch metric circuits, not in the path metric accumulator.

Alternatively, even if, *arguendo*, the branch metric circuit saturation methods and apparatus taught by applicant were viewed as a way to normalize the path accumulators (which may be what the Examiner has in mind), the present solution, again, is markedly different from that disclosed by Bree, as further demonstrated below. In accordance with one embodiment of the present invention, illustrated in Fig. 16 below, the add-compare-save circuitry (ACS) is modified to force a saturation value as the branch metric, as follows.

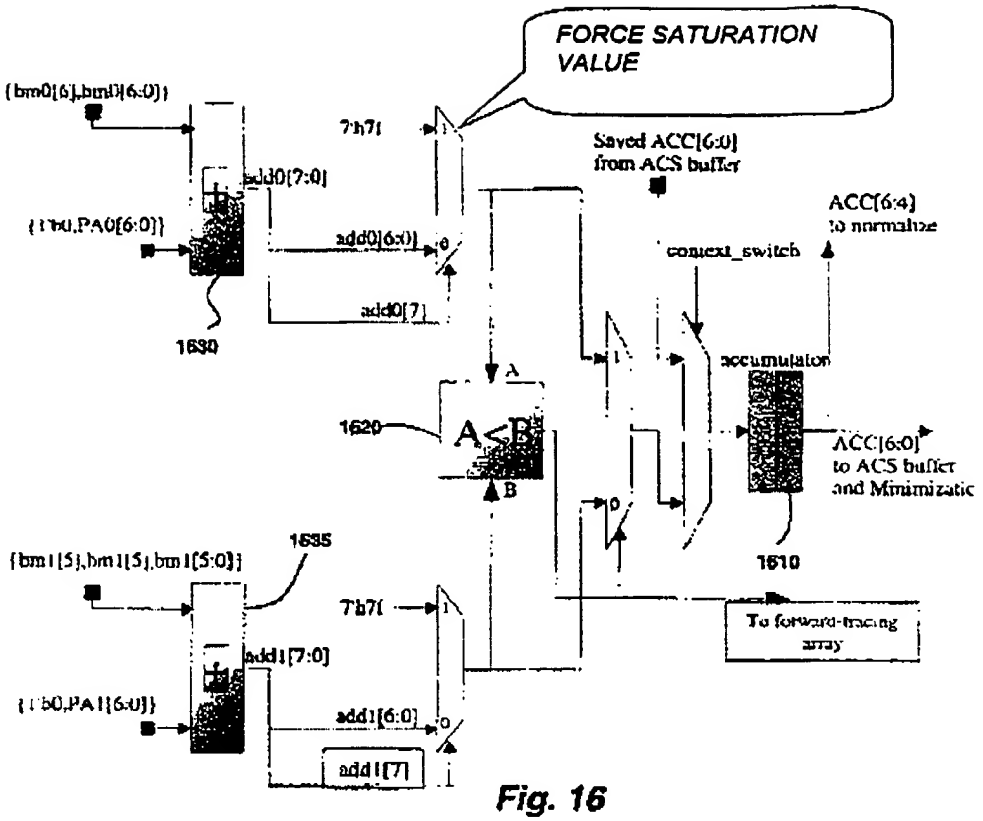

Fig. 16

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In the upper left, a branch metric bm0 is added to a path metric accumulator value, with the resulting sum labeled "add0[7:0]". The msb (sign bit) of that sum, namely add0[7] is used to control the mux to replace the actual sum add0[6:0] with a predetermined saturation value 7'h7f instead. Note, the bubble caption "*Force Saturation Value*" is added here for convenience; it is not part of the actual drawing figure. The specification explains:

"[W]hen all state accumulators exceed a pre-set threshold (e.g., 32, 48), a constant value is subtracted from all of them to avoid overflow. This may be achieved by the normalization process in branch metric unit 1325. In addition, in one embodiment, the ACS adders 1630, 1635 use saturating logic to avoid overflow effects...". Page 55, lines 5-9.

As explained at pages 55-56, the msb is used to detect overflow of the adder (e.g. 1630). In that event, a saturation value (e.g. all 1's) is selected (via mux) in place of the branch metric value. This is realized, in the illustrated embodiment, by a multiplexer. The

saturation logic is variously reflected in claims 1-27. This method and apparatus are not shown in the reference, nor is the present invention obvious in view of Bree.

2. Normalizing the Path Metric Accumulators

In accordance with the present invention, the path metric accumulator (1610 in one embodiment, see Fig. 16) is not normalized by clearing the msb, as taught by Bree et al. Rather, when a normalize control signal is asserted (Normalization Signals 1550 in one embodiment below), the accumulators are normalized *indirectly*. That is, in a preferred embodiment, a selected *normalization value is added to the current branch metric*. For example, see Fig. 15 below:

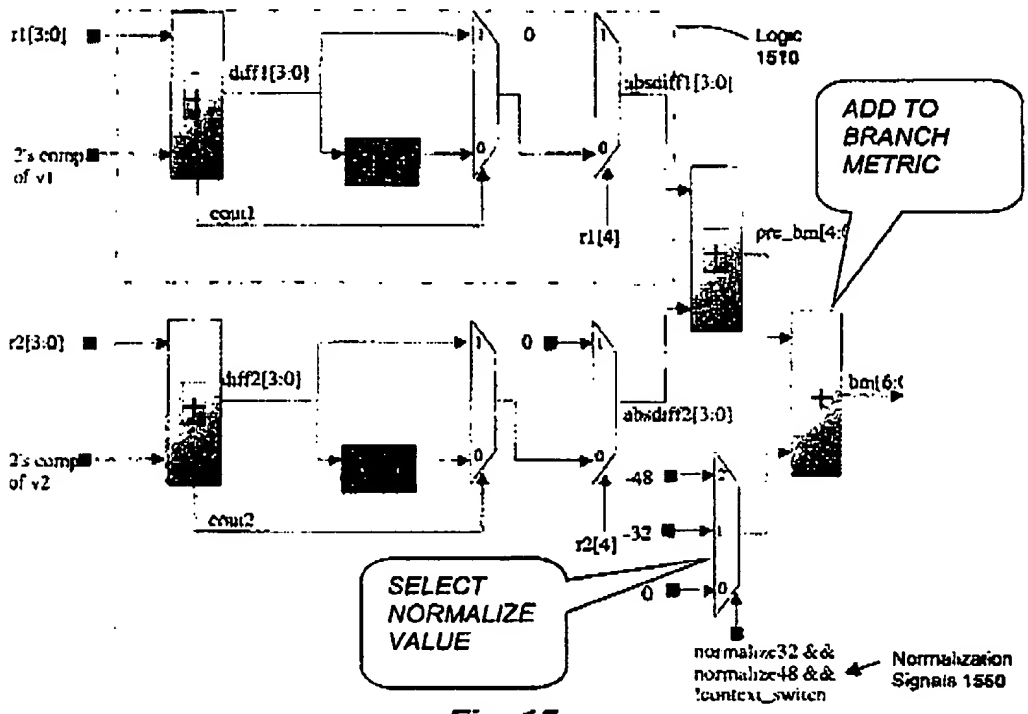

Fig. 15

As illustrated in the embodiment of Fig. 15, the normalization signal selects a normalization value via a multiplexer, e.g. {-48, -32, 0}. Note: the bubble caption "Select

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Normalize Value" is added here for clarity; it is not part of the actual original drawing figure. (The 0 value is a special case not pertinent here.) The selected normalization value is added to the branch metric. See mux "Add to Branch Metric" above (again the bubble caption is added to the drawing for this discussion). In other words, the normalization logic changes the branch metric before it is input to the ACS/ path accumulator. The specification says:

"When normalization is signaled, the set of constants used to calculate the distance metrics at the branch metric units 1325 are switched and replaced by a different set of constants that incorporates the normalization amount... the normalization + distance values, supplied to all ACS accumulators as part of the branch calculation process, will normalize the accumulators simultaneously". Page 53, lines 3-8.

Bree et al. neither disclose nor suggest normalizing the path metric accumulator values by inputting a normalization value to each of the path metric accumulators with a corresponding branch metric value, so that the first normalization value is added to the path metric accumulator value. To the contrary, Bree simply teaches clearing a bit directly in the PMV shift register. For at least these reasons, new claims 28- 36 are patentable over the prior art.

3. Selectable Normalization Values

The present invention has the additional benefit of enabling multiple, selectable normalization amounts, which also is not suggested in the prior art. (Bree simply teaches clearing an MSB bit in a PMV register.) As explained in the specification:

> "Different normalization amounts may be specified, depending on the particular embodiment. For example, in one particular embodiment, illustrated in FIG. 15, "Normalize32" and "Normalize48" signals 1550 received by the branch metric unit 1325 indicate that the branch metric values need to be reduced by the normalization amounts of 32 or 48, respectively, resulting in branch metric values ranging from -48 to +30. ... It should be noted, however, that various other normalization values may be employed while still complying with the underlying principles of the invention."

See page 53 and Fig. 15 above. This feature is reflected, for example, in new claims 28 *et seq, viz*:

28. (New) A method for use in a digital decoder comprising the steps of:
determining a branch metric value;
monitoring a path metric accumulator value;
responsive to the path metric accumulator value reaching a first predetermined value, normalizing the path metric accumulator value by:
selecting a normalization quantity;
providing the selected normalization quantity as an input to the path metric accumulator ...
[emphasis added.]

The specification further discloses:

> "Additional levels of normalization may be used depending on the system configuration. For example, in one embodiment, three normalization signals, norm_hi, norm_med, and norm_low may be used to subtract three different amounts from the accumulators (i.e., depending on the values of each of the accumulators). Normalization signal selection may be accomplished by monitoring the 3 most significant bits of all the state metrics. For example, in one embodiment, if the accumulator values range from N:0, then norm_hi is generated if bit N of all state metrics are set. Norm_med is generated if bit N or bits N-1 and N-2 of all state metrics are set and norm_low is generated if bit N or bit N-1 of all state metrics are set. The constants may be calculated based on the value of N. For example, if norm_hi is set, then all state metrics may be subtracted by 2.sup.N; if norm_med is set then all state metrics may be subtracted by 2.sup.N-1+2.sup.N-2; and if norm_lo is set, then all state metrics may be subtracted by 2.sup.N-1." Page 54.

As noted, Bree simply clears a bit directly in the PMV shift register. There can be no selection among multiple or adjustable normalization signals or values as taught by the present application. The new claims emphasize these features.

The present application is now in condition for allowance. The Examiner is encouraged to telephone the undersigned if any issues remain.

Respectfully submitted,

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